

General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. It is suitable for automotive application.

Features

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

Application

- BLDC Motor driver
- DC-DC
- Battery protection

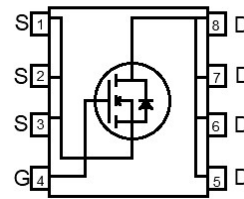
Ordering Information:

Part NO.	ZMSA055N04HN
Marking	ZMS055N04H
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

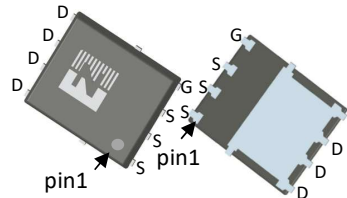
Absolute Maximum Ratings ($T_C=25^\circ\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage ^①	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	68	A
	I_D	$T_C=75^\circ\text{C}$	63	A
	I_D	$T_C=100^\circ\text{C}$	55	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	272	A
Total Power Dissipation	P_D	$T_C=25^\circ\text{C}$	71	W
Total Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3.0	W
Operating Junction Temperature	T_J		-55 to +175	$^\circ\text{C}$
Storage Temperature	T_{STG}		-55 to +175	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	40	mJ
		$L=0.5\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	84	mJ
ESD Level (HBM)	CLASS 1C			

Product Summary



$V_{DS} = 40\text{V}$
 $R_{DS(ON)} = 5.5\text{m}\Omega$
 $I_D = 68\text{A}$



DFN5*6



•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	2.1	°C/W
Thermal resistance, junction-ambient	$R_{thJA}^{②}$		-	50	°C/W
Soldering temperature (total time<10s)	Tsold		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2.0	2.7	4.0	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=40V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=14A$		5.5	6	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=4A$		7		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=14A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	908	-	pF
Output capacitance	C_{oss}		-	244	-	
Reverse transfer capacitance	C_{rss}		-	10	-	
Gate Resistance	R_g	$f=1MHz$	-	1.2		Ω
Total gate charge	Q_g	$V_{DD}=15V, I_D=20A, V_{GS}=10V$	-	14	-	nC
Gate - Source charge	Q_{gs}		-	3.2	-	
Gate - Drain charge	Q_{gd}		-	3.5	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	5	-	ns
Turn-ON Rise time	t_r		-	10	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	8	-	ns
Turn-Off Fall time	t_f		-	3	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=20V, dI_S/dt=100A/\mu s, I_S=50A$	-	30	-	ns
Reverse Recovery Charge	Q_{RR}		-	21	-	nC

Fig.1 Gate-Charge Characteristics

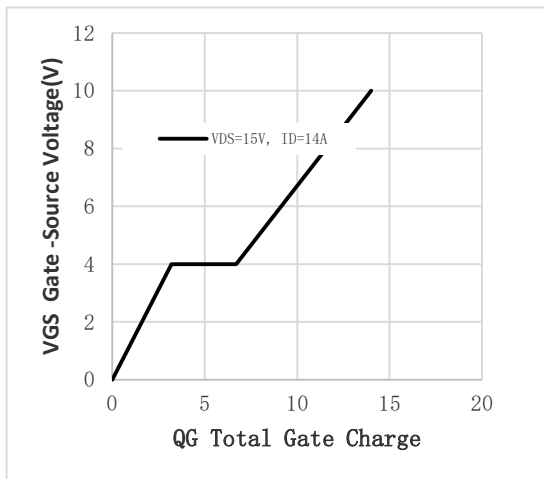


Fig.2 Capacitance Characteristics

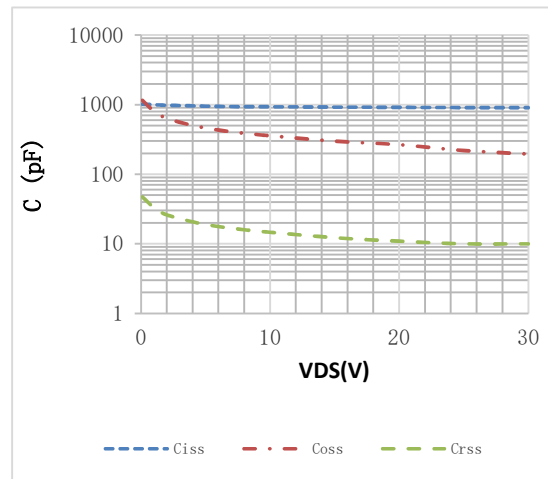


Fig.3 Power Dissipation

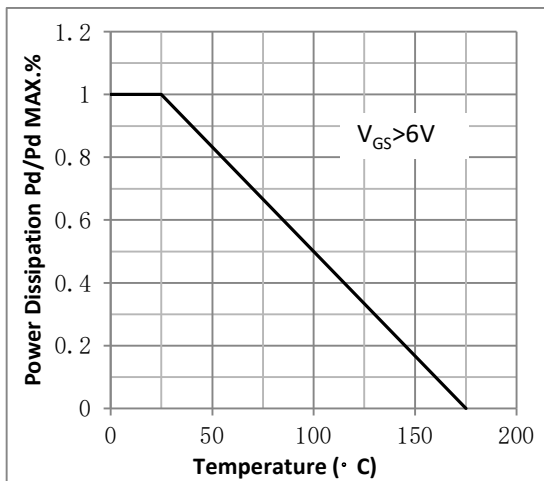


Fig.4 Typical output Characteristics

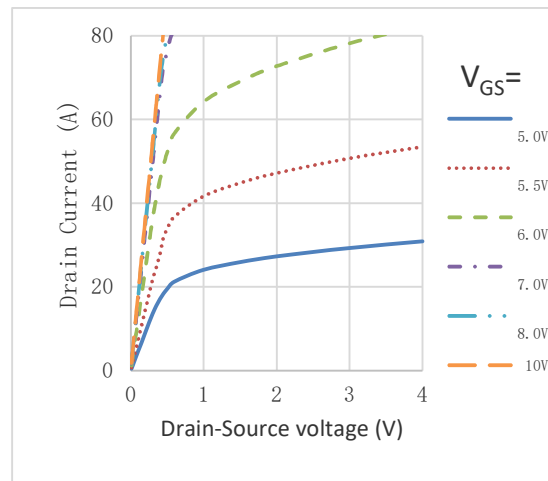


Fig.5 Threshold Voltage V.S Junction Temperature

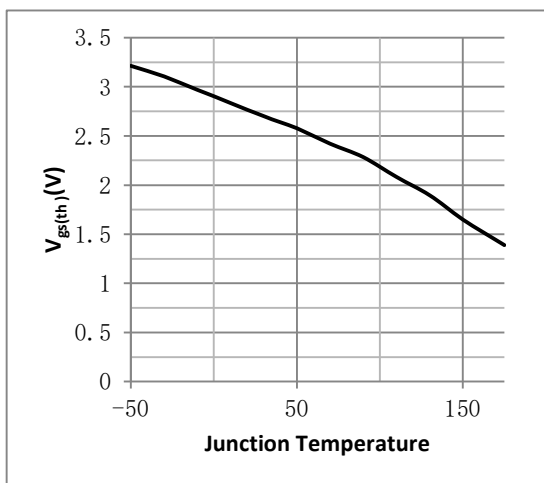


Fig.6 Resistance V.S Drain Current

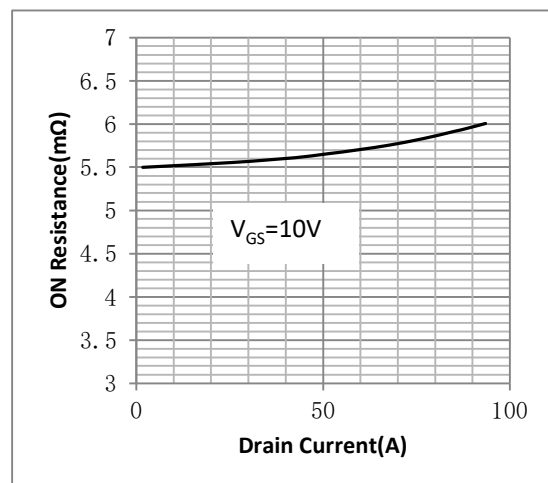


Fig.7 On-Resistance VS Gate Source Voltage

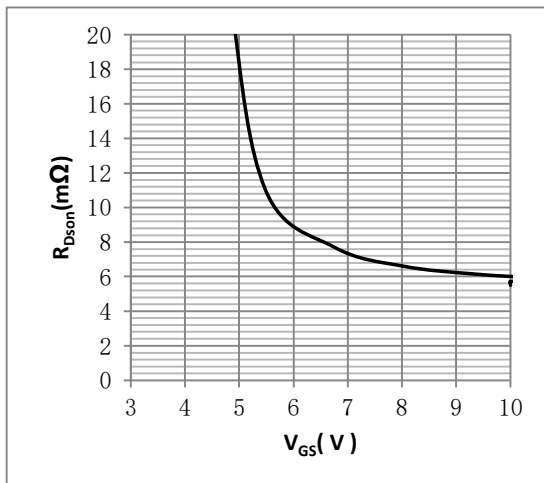


Fig.8 On-Resistance V.S Junction Temperature

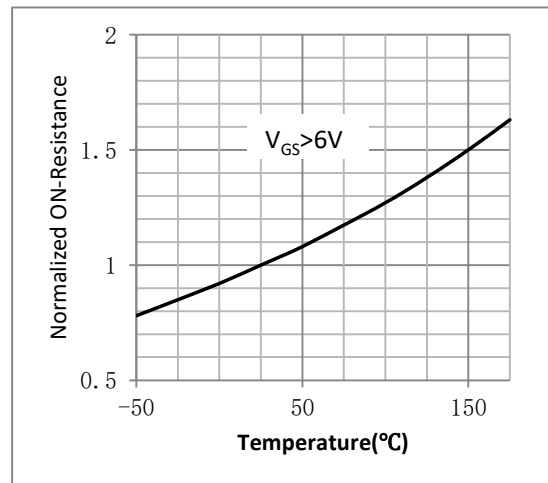


Figure 9. Diode Forward Voltage vs. Current

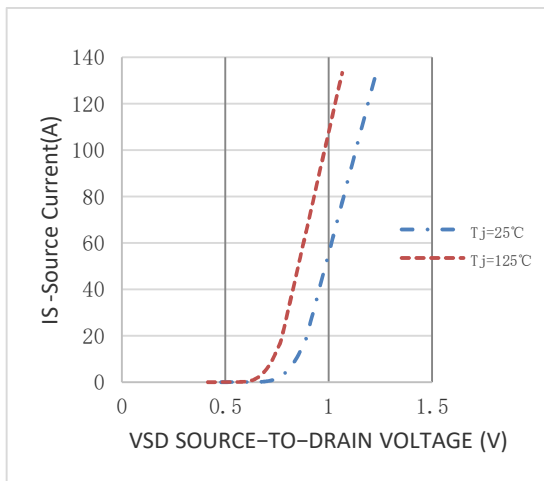


Figure 10. Transfer Characteristics

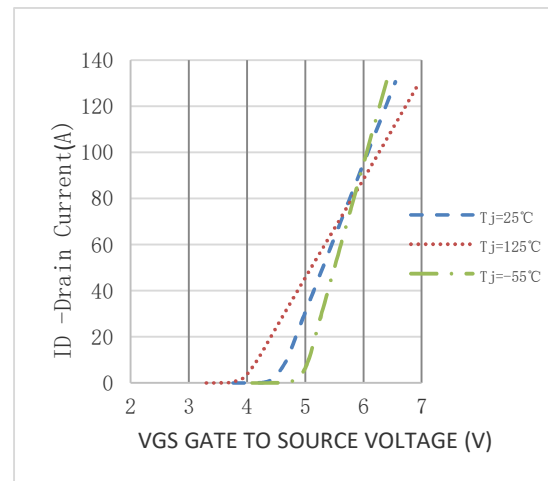


Fig.11 Safe Operating Area

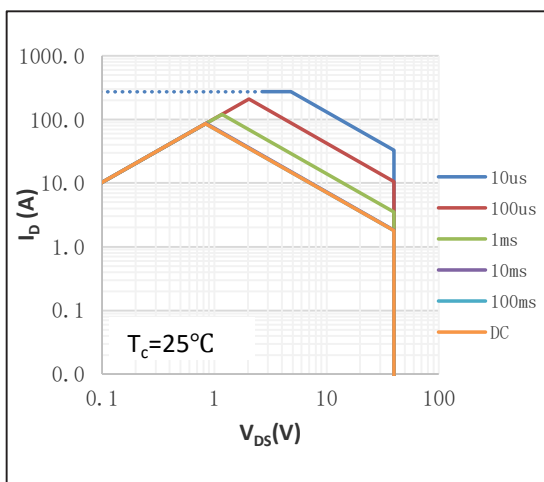
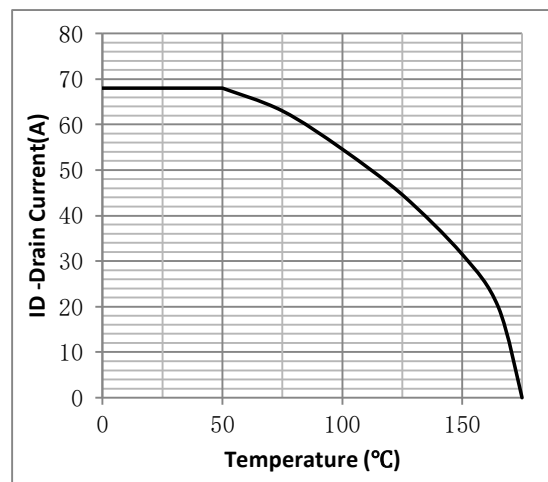
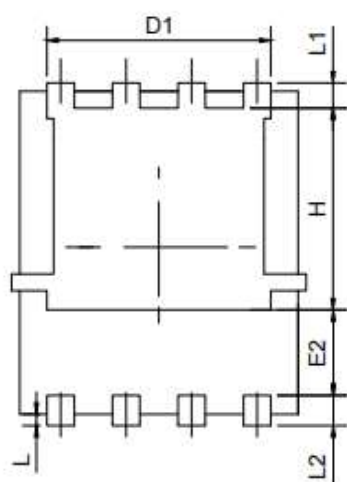
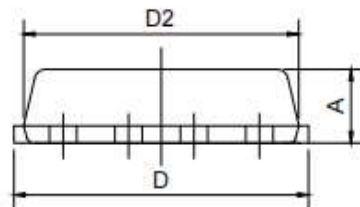
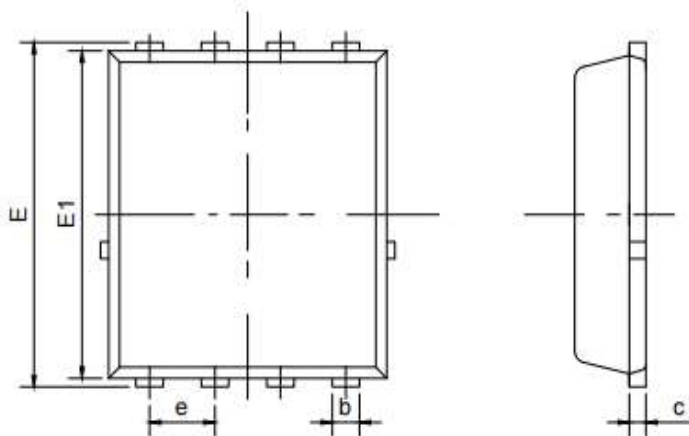


Fig.12 I_D vs. Junction Temperature^③

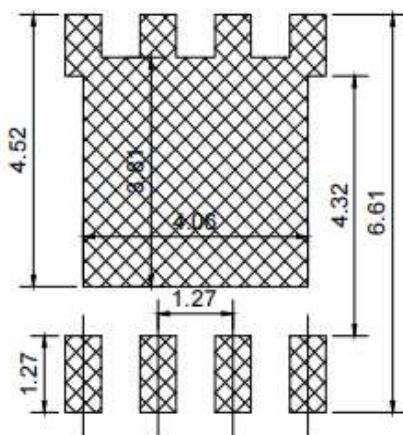


•DFN5*6 Package Outline

1	VMPOD008	DFN5*6 SINGLE PACKAGE OUTLINE SPEC
REV	DRAWING NUMBER	TITLE



Land Pattern
(Only for Reference)



SYMBOLS	COMMON	
	UNIT: mm	
	MIN.	MAX.
A	0.90	1.17
b	0.30	0.51
c	0.15	0.35
D	4.80	5.40
D1	4.00	4.40
D2	4.80	5.00
E	5.90	6.25
E1	5.65	5.85
E2	1.10	-
e	1.27BSC	
L	0.05	0.25
L1	0.28	0.65
L2	0.38	0.71
H	3.30	3.90

Note:

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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Revision History

Version	Date	Change
A	2022.1.6	
B	2022.2.26	1.Add Dynamic characteristic t_f , t_r etc.
C	2022.9.5	1.Add Reach,HF figure,2.ID modify
D	2022.9.19	Change dimension A,L
E	2023.12.19	Correct SOA
F	2024.2.28	Correct package outline dimension
G	2024.8.30	Modified $R_{ds(on)}$ up limit, $i_d@75^{\circ}\text{C}$,100 $^{\circ}\text{C}$
H	2025.1.16	Correct SOA